Adder and Subtractor Unit

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**Introduction**

The purpose of this lab is to learn about the 4-bit adder and subtractor unit and implementing K-maps and a converter to convert 4-bit adder/subtractor outputs to student number representations.

**Results**

Text

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**Figure 1:** VHDL code representing the 4-bit adder/subtractor

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**Figure 2:**  VHDL code representing the converter from 4-bit adder/subtractor to Part B student number K-map

Graphical user interface

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**Figure 3:** VHDL code representing the conversion to a 7seg display

Calendar

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**Figure 4:** The block schematic diagram of Part A

A picture containing timeline

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**Figure 5:** The block schematic diagram of Part B

**Analysis**

In Figure 1, Figure 2, and Figure 3, the VHDL code is show and represents the 3 different symbols that are created and used in this lab. The ASU code was partially copied from the textbook but then modified to function like a 4-bit adder and subtractor. Same with Figure 3, the 7-seg code was copied from the textbook and modified to display what was required in the lab manual. In Figure 2 however, the code was original and was made for the sole purpose of converting its input from the ASU to the 7-seg given the Boolean equations from K-maps with our student numbers as outputs. Figure 4 shows Part A of the lab where a simple ASU is attached to the 7-Seg decoder. Figure 5 shows the same schematic in Figure 4 except with the implementation of the combinatorial symbol with the purpose of converting its input from the ASU to the 7-seg given the Boolean equations from K-maps with our student numbers as outputs. The waveform in this lab, however, did not work out for me as I tried to run it with a simple 1111 + 0000 and the circuit would not return me anything. The waveform simply would not run and would not return a reason why even with creating a completely new circuit in a different directory and trying to redo pin assignments. Everything was tried and no ways worked. Unfortunately, this lab is incomplete but the explanation above along with all the VHDL code and schematic screenshots should be able to display my learning and that I do understand the concepts of an ASU and the implementation of it.